

10/581555

Atty. Dkt. No. 040373-0389

WP20 Rec'd PCT/PTO 02 JUN 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Shinichi HORI

Title: VARIABLE GAIN VOLTAGE/CURRENT CONVERTER CIRCUIT
HAVING CURRENT COMPENSATION CIRCUIT FOR
COMPENSATING FOR CHANGE IN DC CURRENT FLOWING
INTO ACTIVE ELEMENT FOR PERFORMING
VOLTAGE/CURRENT CONVERSION

Appl. No.: Unassigned

International Filing Date: 09/15/2004
371(c) Date: 06/02/2006

Examiner: Unassigned

Art Unit: Unassigned

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), within three (3) months of the date of entry of the national stage as set forth in 37 CFR §1.491.

RELEVANCE OF EACH DOCUMENT

Document A2 relates to a voltage/current conversion circuit which reduces the current offset of an output current caused by the error of the operation current of a pair of transistors which constitute a differential circuit.

Document A3 relates to a voltage-to-current conversion circuit that supplies a current in proportion to an input voltage.

Document A6 relates to a semiconductor integrated circuit device and A/D conversion circuit in order to provide a current source with a high output impedance, a highly accurate current mirror circuit and an A/D conversion circuit with a high accuracy and low power consumption.

Document A7 relates to voltage control type gain variable amplifier circuit to provide the circuit having good oscillation stability with less distortion by placing a voltage control type attenuator in a feedback path to prevent the loop gain of the feedback loop from being charged by the control voltage.

The relevance of Documents A9 and A11 is described in the present specification.

Documents A1, A4, A5 and A11, listed on the attached PTO/SB/08 was cited as being relevant during the prosecution of the corresponding International application. A copy of the International Search Report is attached setting forth the portion of each document considered relevant by the examiner. An English-language counterpart of the foreign-language documents has not been provided. The absence of a translation or an English-language

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counterpart document does not relieve the PTO from its duty to consider any submitted document (37 CFR §1.98 and MPEP §609). English language abstracts are attached.

Applicant respectfully requests that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

Although Applicant believes that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

Date: June 2, 2006

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By Phillip J. Artale *Reg. No.*
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Registration No. 26,257

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: June 2, 2006 <i>(use as many sheets as necessary)</i>				Complete if Known	
Application Number		Unassigned 40/581555			
Filing Date		09/15/2004			
First Named Inventor		Shinichi HORI			
Group Art Unit		Unassigned			
Examiner Name		Unassigned			
Attorney Docket Number		040373-0389			

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			

UNPUBLISHED U.S. PATENT APPLICATION DOCUMENTS						
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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	A1	JP	2004-266316	A	NEC CORP.	09-24-2004		A
	A2	JP	2000-269751	A	MITSUMI ELECTRIC CO.	09-29-2000		A
	A3	JP	2000-134045	A	TEXAS INST JAPAN LTD.	05-12-2000		A
	A4	JP	08-078973		KANEBO LTD.	03-22-1996		A
	A5	JP	08-032369		MITSUMI ELECTRIC CO.	02-02-1996		A
	A6	JP	06-061859		HITACHI LTD.	03-04-1994		A
	A7	JP	05-283948		NEC IC MICROCOMPUT SYST LTD.	10-29-1993		A

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A8	B.I. MILLER et al., "Strain-compensated strained-layer superlattices for 1.5 μm wavelength lasers," Appl. Phys. Lett. 58(18), May 6, 1991, pp. 1952-1954, 1991 American Institute of Physics.	
	A9	B. PANKIEWICZ, et al., "A field programmable analog array for CMOS continuous-time OTA-C filter applications," IEEE Journal of Solid-state circuits, Vol. 37:2, February 2002, pp. 125-136.	
	A10	T. TSUCHIYA et al., "Large number of periods in highly strained InGaAlAs/InGaAlAs MQW structures grown by metalorganic vapor-phase epitaxy," 11 th International Conference on Indium Phosphide and Related Materials, May 16-20, 1999, pp. 47-50.	
	A11	A 1.5 V 75 dB-Dynamic Range 3 rd -Order G _m -C Filter Integrated in a 0.18 μm Standard Digital CMOS Process," ESSCIRC 2002, pp. 647-650.	

Examiner Signature	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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				Group Art Unit	Unassigned
				Examiner Name	Unassigned
				Attorney Docket Number	040373-0389

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A12	C.P. SELTZER, et al., "Zero-net-strain multiquantum well lasers," Electronics Letters, Vol. 27:14, July 4, 1991, pp. 1268-1270.	

Examiner Signature		Date Considered	
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